Rockwell

10938 and 10939
Dot Matrix Display Controller

DESCRIPTION

The Rockwell 10938 and 10939 Dot Matrix Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (vacuum-fluorescent or LED).

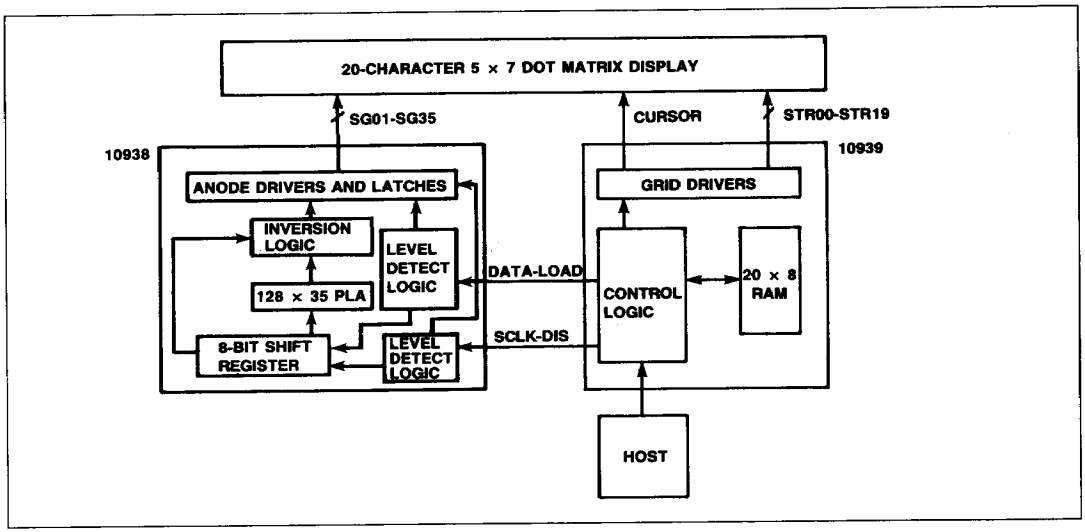
The two-chip set will drive displays with up to 35 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of as many as 80 characters. An internal PLA-type decoder provides character decoding and dot pattern generation for the full 96-character ASCII set and an additional 32 special characters.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range (°C)
10938P	Plastic	0 to +70
10938PE	Plastic	−40 to +85
10939P	Plastic	0 to +70
10939PE	Plastic	−40 to +85

FEATURES

- 20-character display driver cascadable to 80
- Standard 5 × 7 character font.
- Separate cursor driver output
- Direct drive capability for vacuum-fluorescent displays
- 128 × 35 PLA provides segment decoding for full 96-character ASCII set, plus 32 special characters
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- 40-pin DIP

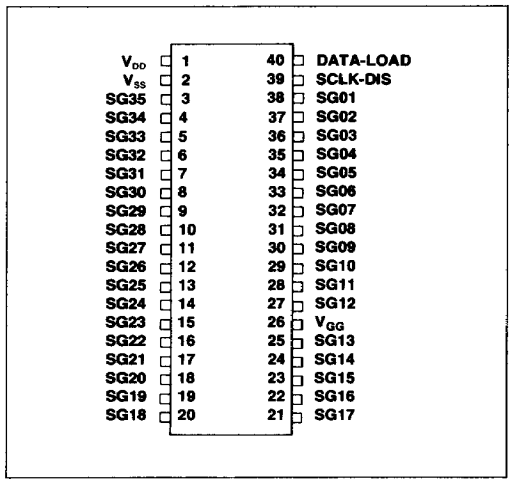


Block Diagram of 10938 and 10939

INTERFACE DESCRIPTION

10938 Pin Functions

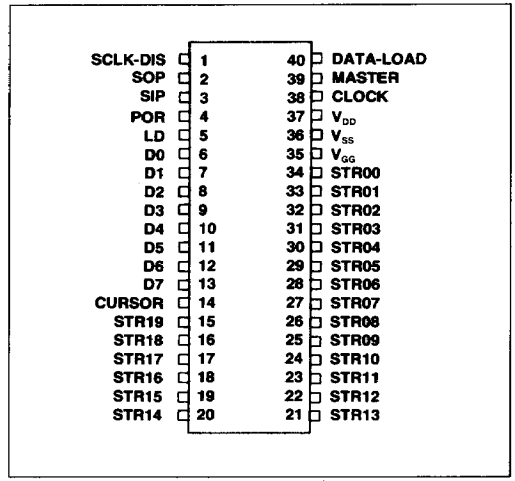
Signal Name	Pin No.	Function
V_{SS}	2	Power and signal reference
SG01-SG35	3-25, 27-38	Anode driver outputs
SCLK-DIS	39	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
V_{DD}	1	DC Power
V_{GG}	26	Display voltage



10938 Pin Configuration

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor drive output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Grid Driver Outputs
V_{GG}	35	Display voltage



10939 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltages are referenced to V_{SS}

Parameter	Symbol	Value	Unit
Operating Temperature			
Commercial	Tc	0 to +70	°C
Industrial	Ti	−40 to +85	°C
Storage Temperature		−55 to +125	°C
Operating Voltage	V_{DD}	−22 to −18	Vdc
Operating Display Voltage	V_{GG}	−50	Vdc

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

All voltages referenced to V_{SS}

Parameter	Notes	Symbol	Min	Typ	Max	Unit
Input D0-D7, LD, SIP	2					
Logic "1"		V_{IH}	−1.2		+0.3	V
Logic "0"		V_{IL}	V_{DD}		−4.2	V
Input POR	2					
Logic "1"		V_{IHPO}	−3.0		+0.3	V
Logic "0"		V_{ILPO}	V_{DD}		−10.0	V
Output SOP	2					
Logic "1"		V_{OHSY}	−1.2		V_{SS}	V
Logic "0"		V_{OLSY}	V_{DD}		−4.2	V
Output Grids, Cursor, and Anodes	1					
Logic "1" (I_{load} = 10 mA 10939, 2 mA 10938)		V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{load} = 0 mA)		V_{OL}	V_{GG}		0.95 × V_{GG}	V

Notes: 1. Designates characteristics for both 10938 and 10939.
2. Designates characteristics for 10939.

OPERATING CURRENTS

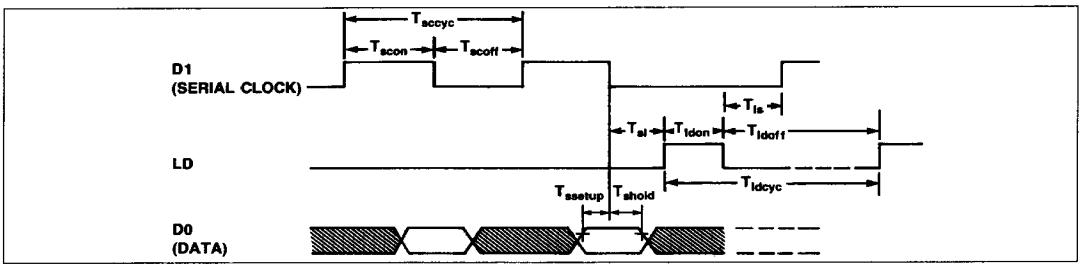
Parameter	Maximum		Typical	Unit
	Industrial TA = −40°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	**Commercial** TA = 0°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	TA = 25°C V_{DD} = −20 Vdc V_{GG} = −50 Vdc	
10938[1]				
I_{DD}	4.5	3.6	3.2	mA
I_{GG}	11.2	9.0	8.0	mA
10939 (master)[2]				
I_{DD}	13.6	10.9	6.0	mA
I_{GG}	1.0	0.8	0.5	mA
10939 (slave)[2]				
I_{DD}	9.1	7.3	4.0	mA
I_{GG}	1.0	0.8	0.5	mA

Notes:
1. The 10938 has 35 internal drivers which are brought out. I_{GG} is proportional to the number of drivers on. The values given are for all 35 drivers on. Divide I_{GG} shown by 35 to determine I_{GG} for one driver.
2. The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle.

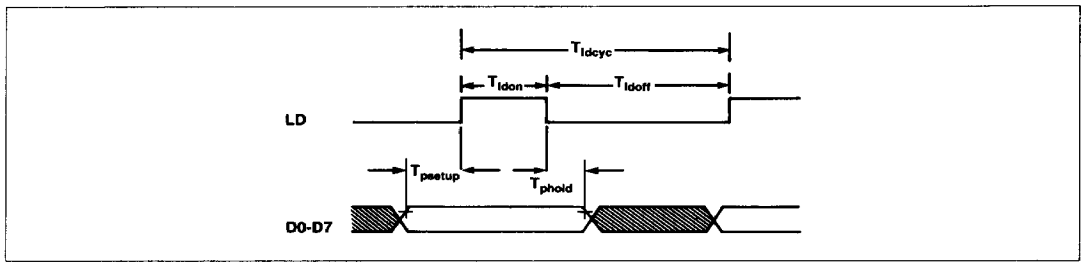
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
GENERAL INTERFACE TIMING					
Data Load (LD)					
On Time	T_{ldon}	1.0			µs
Off time	T_{ldoff}				
Commercial		40.0			µs
Industrial		44.5			µs
Cycle Time	T_{ldcyc}				
Commerical		60.0			µs
Industrial		66.7			µs
SERIAL INTERFACE TIMING					
Serial Clock (D1)					
On Time	T_{scon}	1.0		20.0	µs
Off Time	T_{scoff}	1.0			µs
Cycle Time	T_{sccyc}	2.0			µs
Serial Clock (D0)					
Set-up Time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1.0			µs
LD to Serial Clock	T_{ls}	1.0			µs
PARALLEL INTERFACE TIMING					
Parallel Data (D0–D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

TIMING WAVEFORMS



Serial Interface Timing Waveforms



Parallel Interface Timing Waveforms

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10938/10939 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer as a series of 8-bit words via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10938 to provide the proper timing for the multiplexing operation. A 128 x 35 bit PLA is provided for decoding the full 96 character ASCII set, plus 32 special characters.

The parallel data input mode is implemented by toggling any of data lines D2–D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2–D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. The cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are used to select the operating parameters of the display controller. They must be preceded by a Control Prefix word (0000 0001, hexadecimal 01) to be distinguished from Display Data words.

Buffer Pointer Control

The Buffer Pointer Control code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is used for cursor control only)
09	Enable Blank Mode (data words with MSB = 1 will be blanked and cursor will be on)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed" and cursor will be on)
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10–3F	Not used
40–7F	Load Duty Cycle Register with lower 6 bits (0–63)
80–9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
A0–BF	Not used
C0–D3	Load Buffer Pointer Register with lower 5 bits
E0–FF	Not used

Table 2. Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Note:
DO NOT USE CHARACTER POSITIONS 20–31 (CODES D4–DF)

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Digit Counter Control

The Digit Counter Control code defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Duty Cycle Control code to extend the range of brightness control (see Table 3).

Duty Cycle Control

The Duty Cycle Control code turns the display on and off, adjusts display brightness, and modifies display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Digit Time Control codes (see Table 1). The anode and grid drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off-time. The lower 6 bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 3. Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Digit Time Select

The Digit Time Select code sets the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Table 4. Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

Display Mode Select

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit controls the cursor (see Cursor Control). This bit is known as the data byte control bit. If either Blank or Inverse mode is selected, a "0" in this bit causes a normal character display, while "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to enable Blank Mode, Inverse Mode, or Normal Display Mode.

In the Blank mode, any character with the MSB = "1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Cursor Control

The data byte control bit (MSB 8), besides selecting Blank, Inverse, or Normal mode, also controls the cursor output which is enabled on all characters with the MSB equal to one. Therefore, when the Normal mode is enabled and the MSB of the data byte is set to a one, the normal character is displayed with the cursor on. When the Blank mode is enabled and the MSB is set to a one, the character is blanked but the cursor is on. If Inverse mode is enabled and the MSB is set to a one, the inverse character is displayed and the cursor is on but not inversed.

Start Refresh

At power on, the 10939 is held in an internal halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SOP signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see Control data words 09 and 0A in Table 1). This bit also controls the cursor.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select a character position to be loaded out of sequence, use the Buffer Pointer control code. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed Digit Count.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

a. The Grid Drivers (STR00–STR19) on the 10939 are in the off state.
b. The Anode Drivers (SG01–SG35) on the 10938 are in the off state.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 32.
e. The Buffer Pointer is set to 0.
f. The Digit time is set to 64.
g. The Normal display mode is set.
h. DATA-LOAD is set to high impedance state.
i. SCLK-DIS is set to V_{OL} to disable the anode drivers in the 10938.
j. SOP is set to V_{OL} to disable the sync pulse.

NOTE:

1. When the POR signal is removed, SCLK-DIS is set to the high impedance state.
2. During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD}.

GRID (DIGIT) DRIVERS (STR00–STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display dots will be illuminated when both the Digit Drivers and Dot Drivers for a particular character are energized simultaneously. The cursor segment is generated by the 10939, but its timing characteristics are identical to the anode timing generated by the 10938.

ANODE (DOT) DRIVERS (SG01–SG35)

35 Dot Drivers are provided in the 10938. The output states for each character pattern are internally decoded from the 8-bit characters received from the 10939 by means of a 128 × 35-bit PLA. Data codes and the corresponding patterns are shown in Figure 1. Figure 2 shows the Dot Driver (SG01–SG35) assignments as they relate to the 5 × 7 dot matrix patterns.

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TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10938 and 10939 in a parallel interface with the host system driving a 20 character display. Figure 4 shows a 10938 and a 10939 in a serial interface with the host system driving a 20 character display. Figure 5 shows a 10938 and two 10939's in a parallel interface with the host system driving a 40 character display.

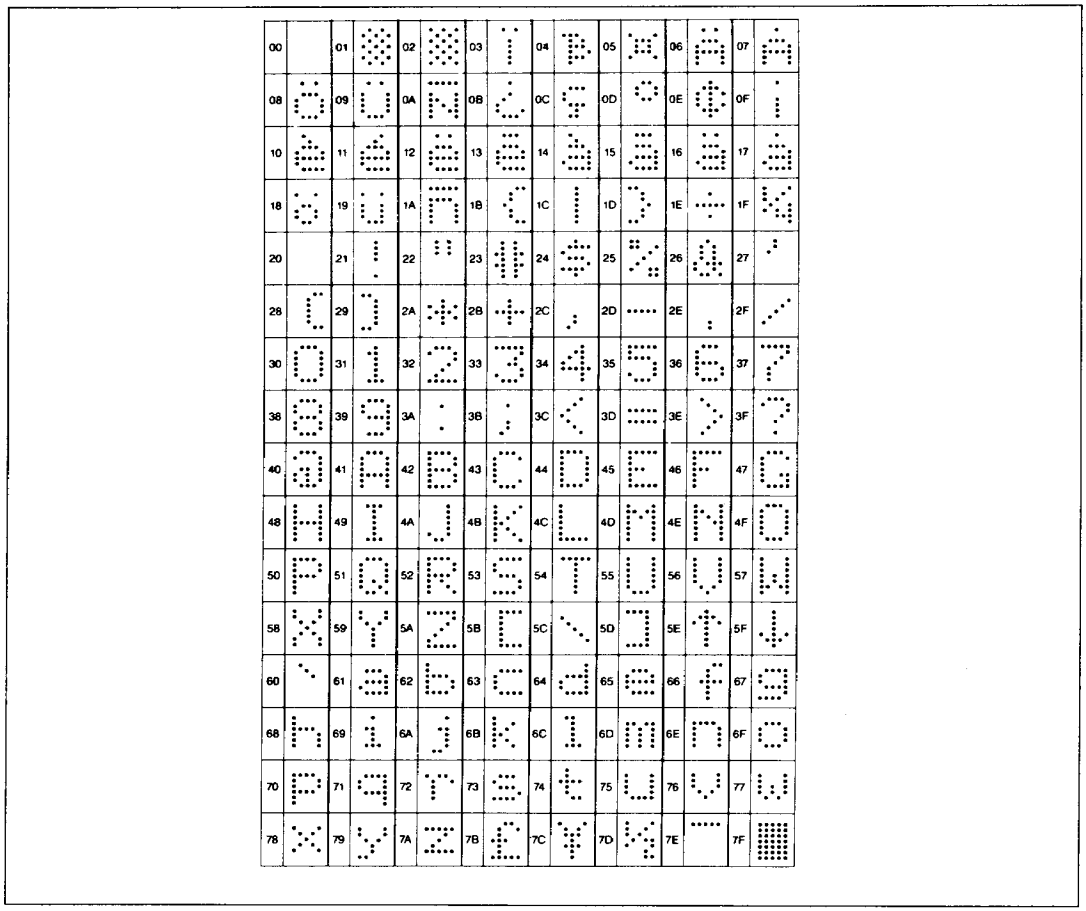

Figure 1. 5 x 7 Dot Matrix PLA Patterns

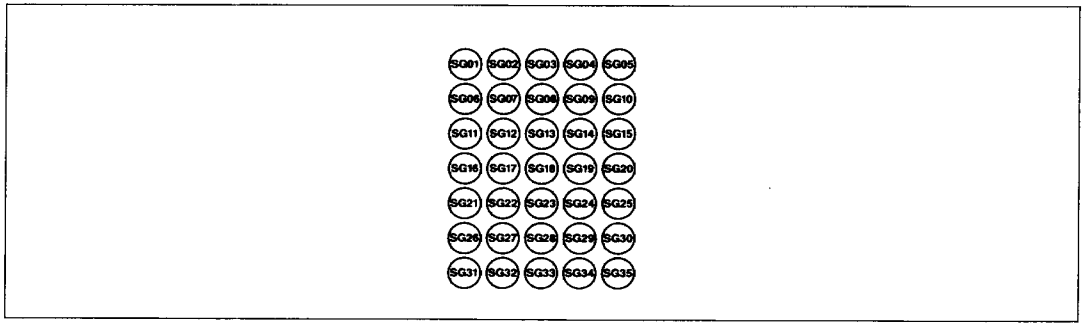

Figure 2. Anode (Dot) Driver Assignments

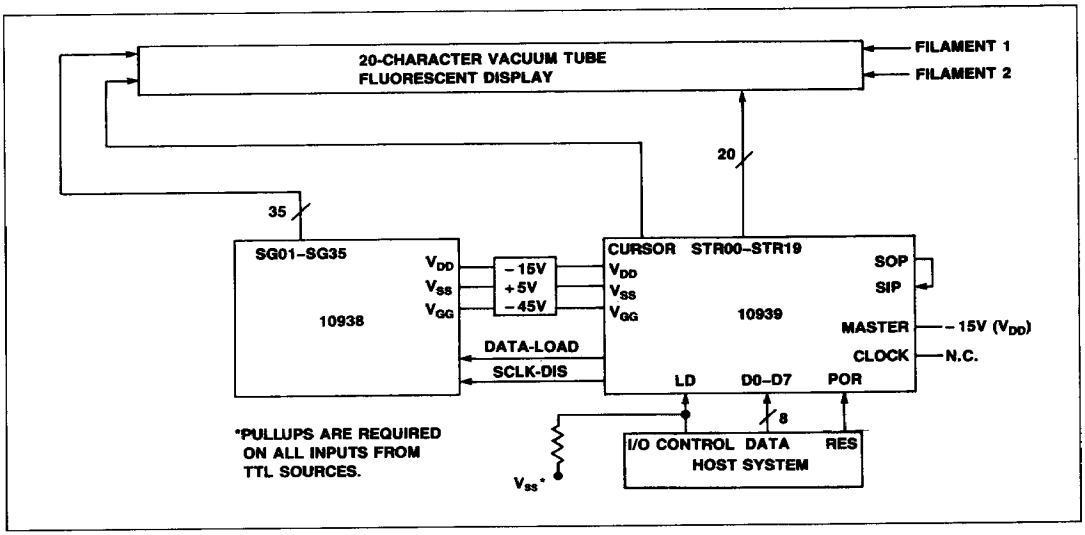

Figure 3. Typical Display System with Parallel Interface to Host System

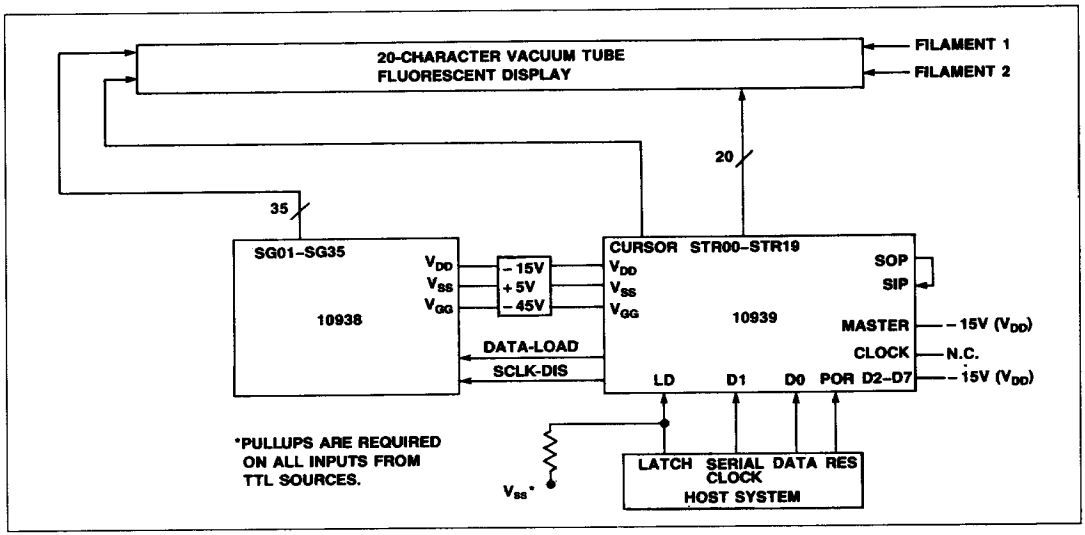

Figure 4. Typical Display System with Serial Interface to Host System

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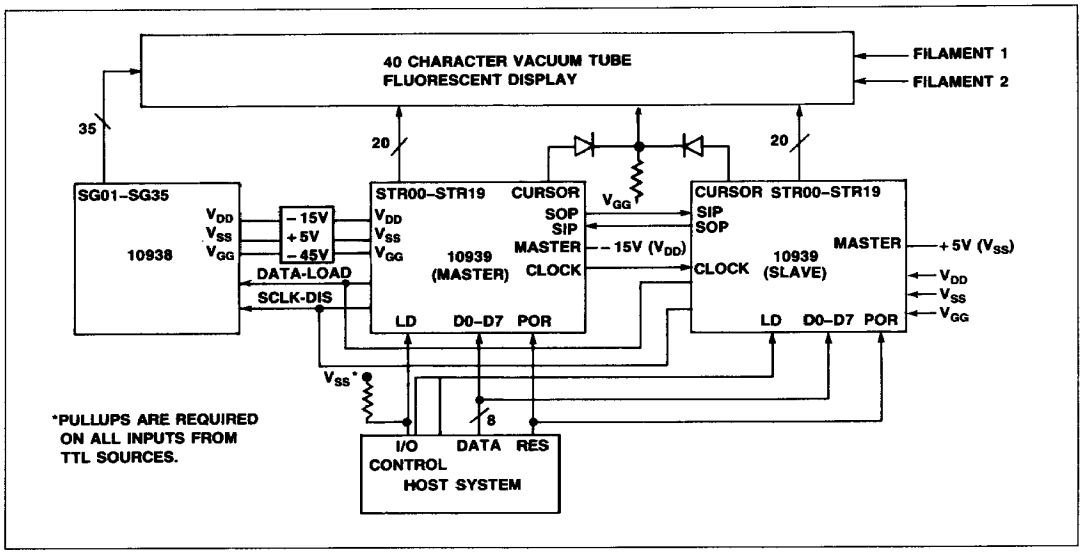

Figure 5. Typical Display System with Parallel Interface to Host and Two 10939 Devices